Abstract

master's degree attestation work

on a theme:

"Research of methods of co-simulationon foundation technologists of VPI"

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The purpose of work

Majority of CADs are already equipped with mixed design tools for some kinds of practical tasks. The Verilog-AMS an VHDL-AMS are the most widespread basic languages for the mixed signals modeling at level near to behavioral, and providing a management the hierarchy of models.

Most systems of mixed modeling are been one or a few programs of analog and digital design with specialized set of external functions for co-operating with other simulators, thus these programs work within the framework of large open infrastructures, created by the leading EDA suppliers.

The mixed design, due to the differences in blocks levels of abstractions, makes it possible to attain a maximal exact design model for every separate block. Accordingly this approach allows form an efficient of working model for complex device on the early stages of planning.

An object of research hired is a number of design algorithms on digital and circuit technology levels which must be linked through additional programmed tools.

By the features of methods of circuit technology design, are qualified by:

- Variable discrete time step;
- The absence of hardly set of the internal states.

The features of digital methods of design automation:

- The event driven modelling;
- The predefined or calculated fixed amount, of internal and output states for complete design and modules.

Each of the design methods has its own problem-oriented language, being either an industry standard or part of requirements to the project, correspondingly. It stipulates difficulties at the use for such tools, as Verilog - AMS/VHDL - AMS, related to the necessary modifications or writing of new models of devices, that increases time on planning, probability of bringing of errors in a model, and also, to the increase in development price.

A presence of the described problems is pre-conditions that the use of digital models in initial language(VHDL/Verilog) and circuit technology models - in problem-oriented language of simulator, at the mixed design is desirable to conduct with minimum interference a man in the underlying structure of initial models. Now for the solution of described problems used:

- modifications of Spice with the built-in kernel of event-driven modeler (for example, X - Spice has the limited support of language of simplified VHDL);
- tools for separate co-simulation of independent CAD/CAM by digital and circuit technology of modeling (NC Verilog/ NC VHDL - Spectre).

Therefore development of an universal interface on the basis of standard of interfacing known VPI can simplify the task of the mixed design modeling for different CAD systems.

Purpose of work

The primary purpose of work is research of methods and tools useful for VPI application in mixed design. Presented number of event-control algorithms for the mixed design, the analysis of which will give the detailed estimation of efficiency of such approach.

Results and conclusions made

- Analysis of requirements to the algorithms of digital design corresponding to tasks of the mixed design;
- Analysis of control tools for simulation process of event-driven design present in different CAD systems;
- Analysis of VPI realizations quality in the different interpreters of Verilog.
- Analysis of management tools by circuit technology CAD systems on the example of Allted;
- Analysis of methods of the mixed design for co-simulation, their applicability to the interfaces of VPI;
- Verification of the considered methods of the mixed design through a standard numeral experiment (DAC, ADC).

Attained results

Key results put in-process, the author presented:

- Comparison of VPI versions in the different Verilog simulators;
- Results of numerical analysis of algorithms of event-drive divided co-simulation realized in interface Modelsim - VPI - Allted;
- Algorithm of for the predefined signals set for the combinatoric logic;
- Cached values changes and reactions usage approach for simulation calls minimization;
- Algorithm of calculation of total dwells for a passive analog block in the process of co-simulation;

- Forming of list of limitations of applicability of tools of VPI for co-simulation within the framework of groups of practical tasks.

Scientific novelty of work

The scientific novelty of work consists in the following:

1) The algorithm of analog-to-digital co-simulation is reworked for VPI/PLI, and differs from initial[1]:
    - The synchronization management in the automatic mode, and predefined from the Verilog modules mode
    - The mechanics of delays storing is offered for passive circuits;
    - The amount of simulation calls decreasing algorithm for VPI/ALLTED is diminished;
2) At first designed co-simulation between the external simulator of Verilog Modelsim and Allted. On the basis of the realizability analysis for different algorithms is conducted by the co-simulation tools of VPI, resulted in-process.
3) Algorithm of automatic ALLTED tasks-file generation for cosimulation tasks.
4) Algorithm of the automatic forming of entrance signal of analog device, on the basis of information, acting from a digital simulator, providing the calculation of delays of distribution of signals in the passive modules of circuit technology косимуляции.

Practical value:

On the basis of the conducted researches the program was written being the platform-independent module for mixed cosimulation Modelsim - VPI - Allted providing the transmission of digital signals through circuit technology DAC.

Conclusions and recommendations :

At the end of the work the conclusions and recommendations set was formed:

- Application of VPI for the decision of tasks in a modern event CADD becomes complicated by not complete realization separate CADD of requirements of standard, by the features of realization of internal planners of events of simulators.
- Development of methods of synchronization in the modern systems event characterized акценторванием attention to the questions of simplification of successive threads and by expansion of introduction многопоточной up-diffused косимуляции. Thus a competition goes between two approaches: by asynchronous synchronization of threads and complication of algorithms of planners of times of synchronization.
- During realization of separate косимуляции as a main problem of the system the height of amount of mutual calls of simulators comes forward with the height of bit

and amount of general signals. For reduction of number of calls next recommendations are formed:

- Application of run-time method of synchronization, which provides the least of cycles of synchronization and even partition of load between simulators;
- Use of buffers of history of reactions on changes which provide reduction of number of surplus calls for passive charts without bringing of distortions in work of device on the whole;
- Forming of proactive signals for a circuit technology simulator, on the basis of information of turn of events and probabilistic analysis of signals;
- To use as a mechanism of exchange reports system events, hardly tied only to the moments of time and concrete changes of signals, that provides reduction of number of calls of procedures of synchronization/of type of data conversion.

The work contains 104pages, 13 images, 21 sources.

Keywords: VERILOG, VPI, ALLTED, CO-SIMULATION, SINHRONIZATION, PLI, MODELSIM, SPICE, XSPICE, LSIM, SABER, PACSIM